IN THE CLAIMS

Claims 1-31 (Canceled)

32. (New) A nonvolatile memory comprising:

a controller;

a plurality of latch circuits;

a plurality of bit lines;

a plurality of word lines; and

a plurality of memory cells,

wherein each of said memory cells has a first terminal and a second terminal,

wherein each of said word lines couples to said first terminals of corresponding ones of said memory cells,

wherein each of said bit lines couples to said second terminals of corresponding ones of said memory cells in parallel, and couples to a corresponding one of said latch circuits,

wherein said memory cells coupled to one word line include first ones and second ones,

wherein said first ones have already stored first data therein, and each of said first ones has one of a first state and a second state according to said first data,

wherein all of said second ones have said first state, and

wherein in programming memory cells, said controller controls selection of a word line, setting of said first data to said latch circuits coupled to said first ones via one of said bit lines, setting of second data to said latch circuits coupled to said second ones, and supplying of a program voltage to said selected word line for storing said second data to said second ones coupled to said selected word line, said first ones remaining with said first data stored therein.

33. (New) A nonvolatile memory according to claim 32,

wherein after said programming, each of said first ones has one of said first state and said second state according to said first data, and each of said second ones has one of said first state and said second state according to said second data.

34. (New) A nonvolatile memory according to claim 33,

wherein each of said memory cells has a threshold voltage within one of a first threshold voltage range and a second threshold range, said first threshold voltage range

corresponding to said first state and said second threshold voltage range corresponding to said second state, and

wherein said programming moves the threshold voltage of said second ones coupled to said selected word line to one of said first threshold voltage range and said second threshold voltage range according to said second data.

35. (New) A nonvolatile memory according to claim 34,

wherein a higher limit voltage of said first threshold voltage range is lower than a lower limit voltage of said second threshold voltage range.

36. (New) A nonvolatile memory according to claim 35,

wherein said first threshold voltage range corresponds to an erase state and said second threshold voltage range corresponds to a program state.

37. (New) A nonvolatile memory comprising:

a controller;

a plurality of bit lines;

a plurality of word lines; and

a plurality of nonvolatile memory cells,

wherein each of said memory cells has a threshold voltage within one of a plurality of threshold voltage ranges, including a first threshold voltage range corresponding to an erase state and a second threshold voltage range corresponding to a program state, and has a first terminal, a second terminal and a well region,

wherein each of said word lines couples to said first terminals of corresponding ones of said nonvolatile memory cells,

wherein each of said bit lines couples to said second terminals of corresponding ones of said nonvolatile memory cells in parallel,

wherein said nonvolatile memory cells coupled to one word line include first ones and second ones,

wherein each of said threshold voltages of said first ones are within either said first threshold voltage range or said second threshold voltage range according to stored first data,

wherein all of said threshold voltages of said second ones are within said first threshold voltage range,

wherein said well regions of adjacent memory cells coupled to one word line are connected together, and

wherein said controller controls, in response to receiving a first command with a second data, selection of one word line, and supplying of a first voltage to said selected word line for changing the threshold voltage of said second ones from said first threshold voltage range to either said first threshold voltage range or said second threshold voltage range according to said second data, the threshold voltage of said first ones remaining in either said first threshold voltage range or said second threshold voltage range according to said first data.

38. (New) A nonvolatile memory according to claim 37,

wherein said controller controls, in response to receiving a second command, selection of one word line and supplying of a second voltage to said selected word line for changing each threshold voltage of said first ones and second ones to be within said first threshold voltage range.

39. (New) A nonvolatile memory according to claim 38, further comprising a plurality of latch circuits,

wherein each of said latch circuits couples to a corresponding bit line,

wherein said controller controls setting of a flag to said latch circuits coupled to memory cells objected to change threshold voltage from said first threshold voltage range to said second threshold voltage range before supplying said first voltage to said selected word line.

40. (New) A nonvolatile memory according to claim 39, wherein said controller controls changing of threshold voltages of memory cells, said threshold voltages being within said second threshold voltage range, to within an intermediate range between said first threshold voltage range and said second threshold voltage range before supplying said first voltage to said selected word line.